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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/760,741	01/17/2001	Jerry M. Brooks	M4065.0374/P374	5786

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WASHINGTON, DC 20037-1526

EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/760,741	BROOKS, JERRY M.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 4 - 21 and 32 - 42* is/are pending in the application.

4a) Of the above claim(s) *32 - 39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4 - 21 and 40 - 42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on October 15, 2003 has been received and entered in the case.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a combined structure that contains the following limitations in claims 40 and 41, a "first cavity ... between the support structure and the first semiconductor die" being formed under the "second cavity ... between the first semiconductor die and the second semiconductor die" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 41 is objected to because of the following informalities:

Claim 41, line 4, "first" [sic: second].

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 41 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In claim 41, the specification fails to disclose the combined structure of claims 41 and 40 that an element "second cavity" in claim 41 is formed on top of the "first cavity".

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 5 – 7, 10, 12, 40 and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Doi et al. '566.

Regarding claim 1, Doi et al. discloses in e.g., Fig. 1, Fig. 2 and column 5, lines 39 - 42 a semiconductor assembly comprising:

- a support structure (20) having a top surface, wherein said support structure is a film; and
- at least one semiconductor die (10) having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said support structure, said at least one semiconductor die (10) being secured at its bottom surface to said top surface of said support structure by a flowable adhesive material (40) which does not extend past any one of the sides of said perimeter of said at least one semiconductor die.

Regarding claim 5, Doi et al. discloses in e.g., column 5, lines 39 - 42 an adhesive material being an epoxy.

Regarding claim 6, Doi et al. discloses in e.g., Fig. 1, Fig. 2 and column 5, lines 39 - 42 said flowable adhesive material (40) covering an area less than or equal to "about" 90% of said at least one semiconductor die bottom surface area.

Regarding claim 7, Doi et al. discloses in e.g., Fig. 6 and column 5, lines 39 - 42 said flowable adhesive material covering an area greater than or equal to "about" 50% of said at least one semiconductor die bottom surface area.

Regarding claim 10, Doi et al. discloses in e.g., Fig. 2 said at least one semiconductor die being in electrical communication (30) with at least one electrical contact area (at the area of the element 80) provided on said support structure.

Regarding claim 12, Doi et al. discloses in e.g., Fig. 2 said at least one electrical contact area being a bonding pad (80).

Regarding claim 40, Doi et al. discloses in e.g., Fig. 1, Fig. 2 and column 5, lines 39 - 42 a semiconductor assembly comprising:

- a support structure (20) having a top surface; and
- a first semiconductor die (10) having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said support structure, said first semiconductor die (10) being secured at its bottom surface to said top surface of said support structure by a compressed flowable adhesive material (40) which does not extend past any one of the sides of said perimeter of said at least one semiconductor die such that there is a first cavity along at least a portion of said perimeter between said support structure and said first semiconductor die, said first cavity being filled with an encapsulating material (42).

Regarding claim 42, Doi et al. discloses in e.g., Fig. 2, Fig. 6 and column 5, lines 39 - 42 a semiconductor assembly comprising:

- a support structure (20) having a top surface; and
- at least one semiconductor die (10) having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said support structure, said at least one semiconductor die (10) being secured at its bottom surface to said top surface of said support structure by a flowable adhesive material (40) which does not extend past any one of the sides of said perimeter of said at least one semiconductor die, said flowable adhesive material covering an area

greater than or equal to "about" 50% of said at least one semiconductor die's bottom surface area.

8. Claims 1, 4 – 7, 10, 12 - 14, 40 and 42 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsumura '874.

Regarding claim 1, Matsumura discloses in e.g., Fig. 1, Fig. 13 and column 6, line 67 – column 7, line 4 a semiconductor assembly comprising:

- a support structure (1) having a top surface, wherein said support structure is a film; and
- at least one semiconductor die (7) having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said support structure, said at least one semiconductor die (7) being secured at its bottom surface to said top surface of said support structure by a flowable adhesive material (5) which does not extend past any one of the sides of said perimeter of said at least one semiconductor die.

Regarding claim 4, Matsumura discloses in e.g., Fig. 1 and Fig. 13 said support structure being at least one semiconductor die with a top and bottom surface.

Regarding claim 5, Matsumura discloses in e.g., column 6, line 67 – column 7, line 4 an adhesive material being an epoxy.

Regarding claim 6, Matsumura discloses in e.g., Fig. 1 and Fig. 13 said flowable adhesive material (40) covering an area less than or equal to "about" 90% of said at least one semiconductor die bottom surface area.

Regarding claim 7, Matsumura discloses in e.g., Fig. 1 and Fig. 13 said flowable adhesive material covering an area greater than or equal to "about" 50% of said at least one semiconductor die bottom surface area.

Regarding claim 10, Matsumura discloses in e.g., Fig. 1 and Fig. 2 said at least one semiconductor die being in electrical communication (15) with at least one electrical contact area (at the area of the element 4) provided on said support structure.

Regarding claim 12, Matsumura discloses in e.g., Fig. 1 said at least one electrical contact area being a bonding pad (4).

Regarding claim 13, Matsumura discloses in e.g., Fig. 1 an encapsulating material (20 and 33) encapsulating the die (7), electrical communication (15) and at least a portion of said support structure (1).

Regarding claim 14, Matsumura discloses in e.g., Fig. 1 said encapsulating material (20 and 33) fills in at least some portion of a space between said bottom surface of said die and said top surface of said support structure.

Regarding claim 40, Matsumura discloses in e.g., Fig. 1, Fig. 13 and column 6, line 67 – column 7, line 4 a semiconductor assembly comprising:

- a support structure (1) having a top surface; and
- a first semiconductor die (7) having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said support structure, said first semiconductor die (7) being secured at its bottom surface to said top surface of said support structure by a compressed flowable adhesive material (5) which does not extend past any one of the sides of said

perimeter of said at least one semiconductor die such that there is a first cavity along at least a portion of said perimeter between said support structure and said first semiconductor die, said first cavity being filled with an encapsulating material (33 and 20).

Regarding claim 42, Matsumura discloses in e.g., Fig. 1, Fig. 13 and column 6, line 67 – column 7, line 4 a semiconductor assembly comprising:

- a support structure (1) having a top surface; and
- at least one semiconductor die (7) having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said support structure, said at least one semiconductor die (7) being secured at its bottom surface to said top surface of said support structure by a flowable adhesive material (5) which does not extend past any one of the sides of said perimeter of said at least one semiconductor die, said flowable adhesive material covering an area greater than or equal to "about" 50% of said at least one semiconductor die's bottom surface area.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doi et al. in view of Takiar et al. '435.

Regarding claims 4 and 11, Doi et al. discloses the claimed invention except for the support structure being at least one semiconductor die and a wire bond. However, Takiar et al. teaches in e.g., Figs. 3, 4 and column 7, lines 62 – 65 a support structure being at least one semiconductor die with a top and bottom surface and an electrical communication being through a wire bond. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Doi et al. by using the semiconductor die for the support structure and wire bond for the electrical communication as taught by Takiar et al. The ordinary artisan would have been motivated to modify Doi et al. in the manner described above for at least the purpose of providing an easy and low cost stacked semiconductor package (column 2, line 28 – column 3, line 25).

11. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doi et al. in view of McMahon '712.

Regarding claims 8 and 9, Doi et al. discloses the claimed invention except for a distance between an electrical contact area and said perimeter of said at least one semiconductor die is less than or equal to about 200 microns. Since McMahon shows in Fig. 5A an electrical contact area (254, at the right-side) extends under the perimeter of a semiconductor die (202), McMahon teaches the following limitation a "distance between an electrical contact area and a perimeter of at least one semiconductor die being less than or equal to *about* 200 microns". Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to

modify Doi et al. by using the distance being less than or equal to about 200 microns as taught by McMahon. The ordinary artisan would have been motivated to modify Doi et al. in the manner described above for at least the purpose of diminishing circuit feature sizes and more power for the semiconductor device (column 1, lines 37 - 48).

12. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doi et al. in view of Fukui et al. '594.

Regarding claim 13, Doi et al. discloses an encapsulating material (42) encapsulating an electrical communication (30) and at least a portion of said support structure (20). However, Doi et al. does not disclose the encapsulating material for encapsulating said die. Fukui et al. teaches in Fig. 1 an encapsulating material (8) encapsulating a die. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Doi et al. by using the encapsulating material to encapsulate the die as taught by Fukui et al. The ordinary artisan would have been motivated to modify Doi et al. in the manner described above for at least the purpose of protecting the die.

Regarding claim 14, Doi et al. discloses in e.g., Fig. 2 said encapsulating material (42) fills in at least some portion of a space between said bottom surface of said die and said top surface of said support structure.

13. Claims 8, 9, 15 - 17 and 19 - 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumura in view of McMahon '712.

Regarding claims 8, 9 and 15, Matsumura discloses in e.g., Fig. 1, Fig. 13 and column 6, line 67 – column 7, line 4 a semiconductor assembly comprising:

- a first semiconductor die (1) having a top and a bottom surface;
- a second semiconductor die (7) having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die (1), said second die (7) being secured at its bottom surface to said top surface of said first semiconductor die by a flowable adhesive material (5) which does not extend past any one of the sides of said perimeter of said second semiconductor die; and
- wherein the top surface of said first semiconductor die has at least one electrical contact area (3) positioned at a location exterior to said perimeter of said second semiconductor die.

Matsumura discloses the claimed invention except for a distance between an electrical contact area and said perimeter of said at least one semiconductor die is less than or equal to about 200 microns. Since McMahon shows in Fig. 5A an electrical contact area (254, at the right-side) extends under the perimeter of a semiconductor die (202), McMahon teaches the following limitation a "distance between an electrical contact area and a perimeter of at least one semiconductor die being less than or equal to *about* 200 microns". Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Matsumura by using the distance being less than or equal to about 200 microns as taught by McMahon. The ordinary artisan would have been motivated to modify Matsumura in the manner

described above for at least the purpose of diminishing circuit feature sizes and more power for the semiconductor device (column 1, lines 37 - 48).

Regarding claim 16, Matsumura discloses in e.g., Fig. 1 said first semiconductor die (1) being secured to a support structure (17).

Regarding claim 17, Matsumura discloses in e.g., Fig. 1 said support structure (17) being a film.

Regarding claim 19, Matsumura discloses in e.g., column 6, line 67 – column 7, line 4 an adhesive material being an epoxy.

Regarding claim 20, Matsumura discloses in e.g., Fig. 1 said flowable adhesive material (5) covering an area less than or equal to "about" 90% of said at least one semiconductor die bottom surface area.

Regarding claim 21, Matsumura discloses in e.g., Fig. 1 said flowable adhesive material covering an area greater than or equal to "about" 50% of said at least one semiconductor die bottom surface area.

14. Claims 11 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumura in view of Takiar et al. '435.

Regarding claims 11 and 41, Matsumura discloses in e.g., Fig. 1 and Fig. 13 a second semiconductor die (9) having a perimeter, including four sides, and a top and bottom surface, said second (for examination purposes) semiconductor die being secured at its bottom surface to said top surface of said first semiconductor die (7) by a compressed flowable adhesive material (5 between 7 and 9) which does not extend past any one of the sides of said perimeter of said

second semiconductor die such that there is a second cavity along at least a portion of said perimeter between said first semiconductor die and said second semiconductor die, said second cavity being filled with said encapsulating material (33 and 20). However, Matsumura does not disclose a wire bond and said bottom surface of the second semiconductor chip having a smaller area than said top surface of said first semiconductor die.

Takiar et al. teaches in e.g., Figs. 3, 4 and column 7, lines 62 – 65 an electrical communication being through a wire bond and a bottom surface of the second semiconductor chip (76) having a smaller area than said top surface of said first semiconductor die (74). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Matsumura by using the semiconductor die for the support structure and wire bond for the electrical communication as taught by Takiar et al. The ordinary artisan would have been motivated to modify Matsumura in the manner described above for at least the purpose of providing an easy and low cost stacked semiconductor package (column 2, line 28 – column 3, line 25).

15. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumura in view of McMahon as applied to claims 15 and 16 above, and further in view of Crowley et al. '147.

Matsumura, as modified, discloses the claimed invention except for the support structure being a printed circuit board. However, Crowley et al. teaches in Fig. 1 and column 3, line 65 – column 4, line 4 a support structure (16) being a printed circuit board. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify

Matsumura by using the printed circuit board for the support structure as taught by Crowley et al. The ordinary artisan would have been motivated to modify Matsumura in the manner described above for at least the purpose of decreasing a thermal expansion between the chip and the support structure.

Response to Arguments

16. Applicant's arguments with respect to claims 1 and 15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Suzuki et al. and Lin disclose a flowable adhesive material between semiconductor devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
12/27/03 3:53:35 PM

B.WILLIAM BAUMEISTER
PRIMARY EXAMINER